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Fabrication of Transferable Al_2O_3 Nanosheet by Atomic Layer Deposition for Graphene FET

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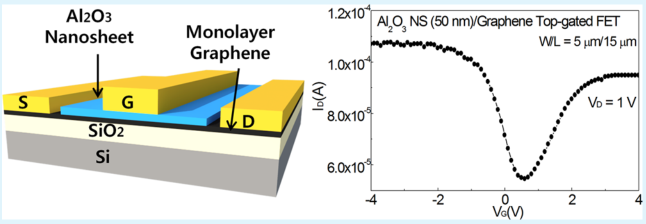
S *Supporting Information*

ABSTRACT: Without introducing defects in the monolayer of carbon lattice, the deposition of high-κ dielectric material is a significant challenge because of the difficulty of high-quality oxide nucleation on graphene. Previous investigations of the deposition of high-κ dielectrics on graphene have often reported significant degradation of the electrical properties of graphene. In this study, we report a new way to integrate high-κ dielectrics with graphene by transferring a high-κ dielectric nanosheet onto graphene. Al_2O_3 film was deposited on a sacrificial layer using an atomic layer deposition process and the Al_2O_3 nanosheet was fabricated by removing the sacrificial layer. Top-gated graphene field-effect transistors were fabricated and characterized using the Al_2O_3 nanosheet as a gate dielectric. The top-gated graphene was demonstrated to have a field-effect mobility up to 2200 $cm^2/(V\ s)$. This method provides a new method for high-performance graphene devices with broad potential impacts reaching from high-frequency high-speed circuits to flexible electronics.



KEYWORDS: *graphene, gate dielectric, atomic layer deposition, Al_2O_3, nanosheet, top-gated field effect transistor*

INTRODUCTION

Since the discovery of graphene in 2004,[1] this single-layer, thin, hexagonal carbon atom structure (one carbon atom thickness is approximately 0.34 nm) with very high mobility (greater than 200,000 $cm^2/(V\ s)$ at 4.2 K for suspended[2]) has drawn attention as a promising material for future nanoelectronics and as a substitute for silicon. In recent years, considerable research has been performed to grow large-area graphene. Wafer-scale graphene has been synthesized[3] and continuous roll-to-roll growth of graphene has been reported.[4] Graphene-based electronic devices may be fabricated using technologies similar to conventional silicon-based electronic devices. To apply conventional technologies to graphene, various studies have been performed; however, some of them could not be directly used to fabricate graphene-based devices. For example, graphene is seriously damaged by the sputtering process, and so it cannot be directly applied to graphene fabrication.[5]

For conventional nanoelectronic devices, atomic layer deposition (ALD) is an appropriate deposition technique for controlled thickness and ultrathin homogeneous films. However, ALD of thin films on graphene is not easy because there are only sp2 bonds and no dangling bonds on the defect-free graphene surface, which are needed for chemical surface reactions. Experimental observation of ALD on graphene also has been performed.[6] Nevertheless, some researchers have been able to deposit thin films, such as HfO_2[7,8] and Al_2O_3,[9,10] on pristine graphene and fabricate top-gated devices with good performance. To deposit smooth, uniform films on graphene, the surface has to be pretreated to produce more dangling bonds, which act as nucleation sites. NO_2 functionalization[11] and ozone treatment[12] have been successfully used in the deposition of thin films on carbon nanotubes;[13,14] other approaches for pretreated graphene have also been applied. For example, a thin (∼1 nm thick) seed layer of evaporated metal was oxidized before ALD[15] or polymer films were used as a buffer layer for ALD.[6] Recently, there have been reports of physically transferred dielectric materials for graphene devices. Duan et al. reported a transfer process of Al_2O_3 nanoribbons using contact printing on exfoliated graphene[16] or top-gate-electrode/dielectric-layer-stacks on chemical vapor deposition (CVD)-grown graphene[17] to produce top-gated graphene field effect transistor (FET). Lee et al. fabricated a physically transferrable Al_2O_3 layer using Cu foil and used it as gate insulator layer of a graphene-carbon nanotube FET.[18] Theses researches demonstrate the production of gate oxide layers using physical bonds instead of chemical bonds, which showed good dielectric characteristics. So they opened a new way for

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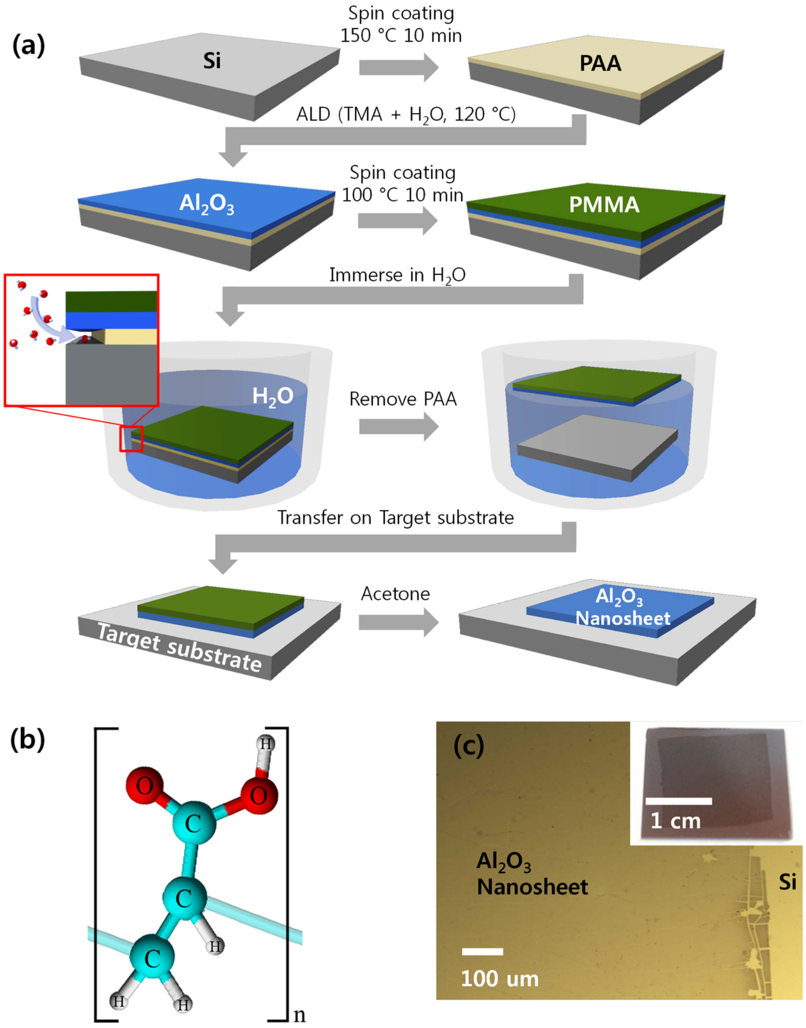


Figure 1. (a) Schematic of the Al_2O_3 nanosheet fabrication process. (b) Chemical structure of poly(acrylic acid). (c) Optical microscope image of the transferred Al_2O_3 nanosheet (30 nm) on the Si substrate (Inset: optical image of the transferred Al_2O_3 nanosheet (30 nm) on a Si substrate).

fabricating devices regardless of materials using conventional equipment.

Here we report the realization of a top-gated graphene FET without any chemical or physical treatments on graphene. A transferrable Al_2O_3 nanosheet (NS) was fabricated using the ALD process and a sacrificial layer. Top-gated graphene FETs using both transferrable Al_2O_3 NS and thermal ALD (Th-ALD) Al_2O_3 on CVD-grown graphene were fabricated for comparison study and their electrical characteristics were investigated.

■ EXPERIMENTAL SECTION

Initially, an water-soluble poly(acrylic) acid (PAA) (Alfa Aesar, molecular weight of PAA = 244 000 g/mol) as a sacrificial layer was formed on the Si substrate by spin-coating and annealed at 150 °C for 10 min under ambient conditions to evaporate the solvents of PAA. After annealing, Al_2O_3 thin film was deposited on the sacrificial layer using a homemade thermal ALD (Th-ALD) at 120 °C with trimethyl aluminum (TMA) and H_2O as precursors of Al and O, respectively. ALD is a kind of CVD process using chemical reaction between hydroxyl groups on the substrates and ligands of the precursor or reactant. However, most of the widely used polymers, such as polyethylene, poly(vinyl chloride) and polystyrene, do not have hydroxyl groups in the chemical structure. So, the mechanisms of ALD on the polymer are adsorption of precursors on the surface or absorption of precursors into the near surface region, which result in nucleation delays of the initial ALD process.[19] Therefore, Al_2O_3 could be deposited on PAA using the ALD process because of the hydroxyl group of PAA. The sample was then covered with poly(methyl methacrylate) (PMMA) as a supporting layer for reducing tearing problems during the transfer process and annealed at 100 °C for 10 min to enhance the adhesion between PMMA and the Al_2O_3 thin film. The solubility of PAA in water facilitated the use of PMMA as a polymer-supporting layer. In Figure 1a, step 4, both top-side (PMMA, the supporting layer) and bottom-side (PAA, the sacrificial layer) of the Al_2O_3 thin film were polymers and both polymers must be removed to obtain Al_2O_3 NS. Acetone cannot be used because it removes both the sacrificial and supporting layers. Therefore, water-soluble PAA was used as the sacrificial layer because water removes only the sacrificial layer. By dipping the sample in water, the sacrificial layer was removed and the Al_2O_3 NS floated on the surface of water and it was scooped up by a target substrate. The supporting layer was then removed using acetone, isopropyl alcohol, and deionized water and then dried with nitrogen gas. The thickness of the Al_2O_3 NS was measured by ellipsometry. The surface morphology and interface between the transferred NS and target substrate were investigated using scanning electron microscopy (SEM) and atomic force microscopy (AFM). The dielectric properties of the transferred Al_2O_3 NS were investigated by preparing Ru/Al_2O_3/p-type Si metal-oxide silicon (MOS) capacitors.

A monolayer graphene was grown using a conventional CVD method at 1000 °C with methane and hydrogen gas. The monolayer graphene was certified using a Raman spectroscopy. Graphene was transferred to a 300 nm silicon oxide and graphene channel was patterned using photolithography and oxygen plasma treatments. On top of the graphene, 50 nm of Al_2O_3 NS was transferred and 50 nm of Th-ALD Al_2O_3 thin film was deposited as gate insulators. To remove water under the Al_2O_3 NS and to enhance adhesion between NS and graphene for reduce peeling problem (see Figure S3 in the Supporting Information), we annealed samples at 200 °C in the vacuum with hydrogen and argon gases for about 30 min. Then, both Al_2O_3 were patterned and etched using photolithography. Finally, source, drain, and top gate electrode (50 nm Ti) of graphene FET were deposited using the evaporation and a lift-off process. The electrical properties of the MOS capacitors and top-gated graphene FETs were measured using a probe station (Keithley 306 electrometer).

■ RESULTS AND DISCUSSION

Figure 1a shows the fabrication process of Al_2O_3 NS using a sacrificial layer and ALD process. The water-soluble PAA, a sacrificial layer in this study, has a hydroxyl group on its chemical structure (Figure 1b) that can act as a nucleation site for the precursor and reactant in the ALD process. Due to the hydroxyl group of PAA, Al_2O_3 thin film was deposited on PAA and Al_2O_3 NS was successfully transferred to the target substrate. An optical microscope image of the transferred Al_2O_3 NS (30 nm) on the Si substrate is shown in Figure 1c. Some cracks and fragments are observed on the edge of the NS (right side of the image); however, the inner part of the NS is quite clean and uniform. A large area and uniform NS is observed in the inset image. The largest size of NS with this process is about 5 cm and minimum thickness is about 7 nm (see Figure S1 in the Supporting Information).

A flat and clean surface of Al_2O_3 NS is observed in the top SEM image (Figure 2a). We especially chose this area for the fine focusing by using a crevice (white line in the image). Overall, the surface has no wrinkles or folded regions. If the surface is not flat and air gaps between the Al_2O_3 NS and graphene are generated during the transfer process, the electrical properties of the devices would be degraded. If there are air gaps between Al_2O_3 NS and graphene, the air gaps would connect in series with Al_2O_3 NS and graphene vertically. As a result, series capacitors with very low permittivity of the air (ε_{air} = 1.0006) would be generated and they would degrade the characteristics of the devices by decreasing the gate capacitance.[18] However, no air gaps are observed between Al_2O_3 NS and the substrate in the cross-sectional SEM image (Figure 2b), indicating the transferred NS is quite flat and successfully transferred to the Si substrate. The flat surface of Al_2O_3 NS is also observed in the AFM image. Figure 3a is an

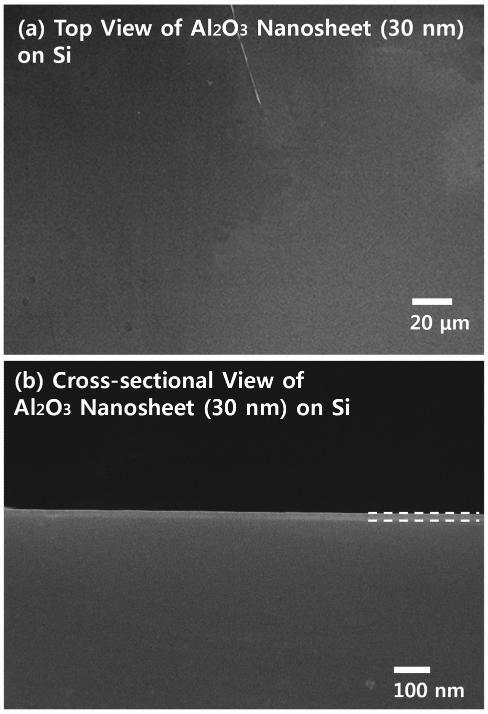


Figure 2. (a) Top and (b) cross-sectional SEM image of the transferred Al_2O_3 nanosheet (30 nm) on a Si substrate.

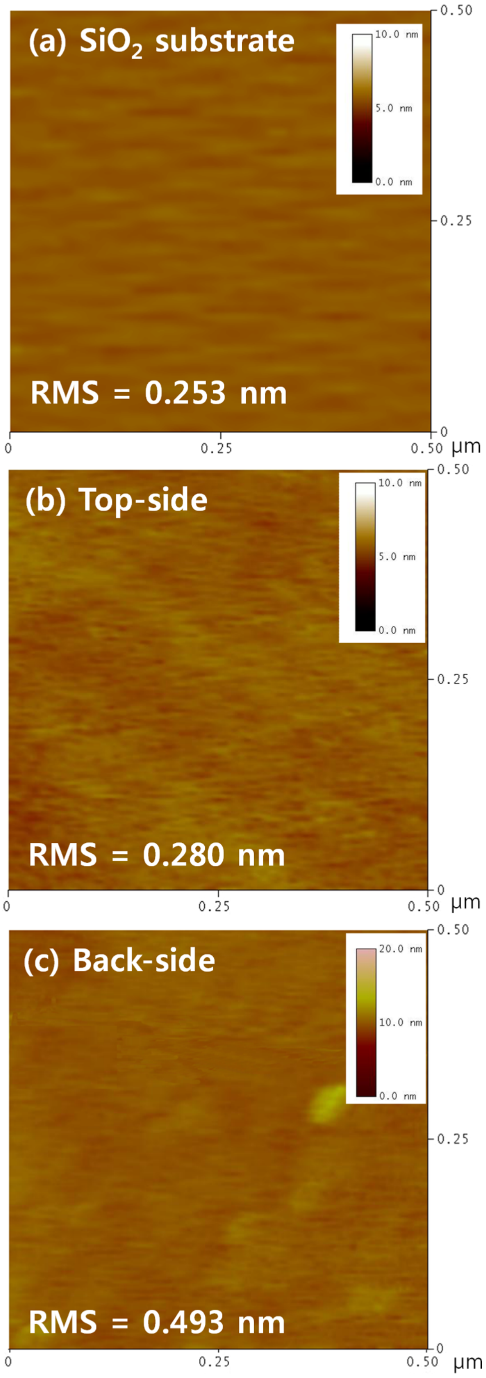
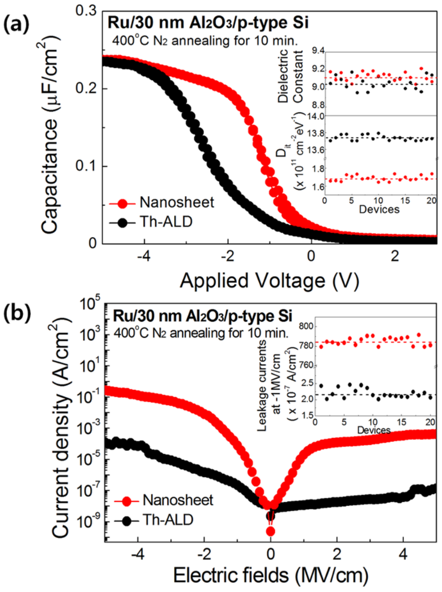


Figure 3. AFM measurements on the (a) SiO_2 substrate, (b) top-side, and (c) back-side of the transferred Al_2O_3 (30 nm) nanosheet on a Si substrate.

AFM image of SiO_2 substrate and it shows very flat with very low root mean square (RMS) roughness about 0.253 nm. Figure 3b is a top-side AFM image of Al_2O_3 NS. The surface of transferred Al_2O_3 NS is very flat with low surface roughness follows by flat SiO_2 substrate and its RMS roughness is 0.280 nm. However, from a previous report of ALD on polymers, the interface between the ALD thin film and some of polymers have a mixed structure of oxide and polymer materials due to the mechanisms of ALD on the polymer.[19] To confirm the interface structure, the back-side of the transferred Al_2O_3 NS is observed using AFM. The back-side of the Al_2O_3 NS samples are prepared using a process similar to the “pick up” method.[20] Al_2O_3 NS floating on the water surface is picked up with the Si substrate. The back-side of the Al_2O_3 NS surface is nearly flat but small dots are observed in Figure 3c. The dots are assumed to be residue of partially melted PAA and these dots have negligible effects on the properties of Al_2O_3 NS because they are very small and the overall back-side surface is also quite flat.

Ru/30 nm Al_2O_3 NS/p-type Si MOS capacitors are fabricated to investigate the electrical properties of Al_2O_3 NS. MOS capacitors using Th-ALD Al_2O_3 on Si are also fabricated for the comparison study. Both samples are annealed at 400 °C in a N_2 condition for 10 minutes. Figure 4 shows the (a) capacitance−voltage (C−V), (b) current−voltage (I−V) curves and (c) a summary of the dielectric properties of transferred Al_2O_3 NS and Th-ALD Al_2O_3. The calculated dielectric constant of Al_2O_3 NS is approximately 9.1 and it is nearly the same as that of Th-ALD Al_2O_3 (dielectric constant 9.0). The interface state density (D_{it}) value of Al_2O_3 NS is 1.69×10^{11} cm^{-2} eV^{-1} and its hysteresis is nearly 0 mV, implying the trap charge density and trapped oxide charges between transferred Al_2O_3 NS and the Si substrate are nearly zero. Therefore, the interface between the Al_2O_3 NS and Si substrate is formed to a clean junction. A negative flat band voltage shift is observed for the Th-ALD Al_2O_3 film, which is caused by positive fixed oxide charges. Some previous studies reported the negative shift of the flat band voltage at low temperature ALD (100−150 °C) of Al_2O_3 films[21,22] and the Th-ALD Al_2O_3 film in this study is also deposited at a low temperature of 120 °C. In Figure 4b, the Al_2O_3 NS shows a slightly larger leakage current than that of Th-ALD Al_2O_3 but its value is quite small and negligible. Al_2O_3 NS has more enhanced dielectric properties than Th-ALD Al_2O_3 film. Al_2O_3 NS has a 10 times lower D_{it} and smaller flat band voltage shift than Th-ALD Al_2O_3 film. The D_{it} and flat band voltage shift are affected by interface-trapped charges and fixed-oxide charges that exist at the interface of the deposited film and substrate, respectively. For Al_2O_3 NS, some opposite charges in the water may be attached to the bottom of NS by columbic attraction during the transfer process, resulting in the suppressing the effects of charges in the films. Finally, they reduce D_{it} and flat band voltage shift. Calculated dielectric constants, D_{it}, and leakage currents for 20 devices are shown in the insets of panels a and b in Figure 4. They imply that Al_2O_3 NS and Th-ALD Al_2O_3 films have quite good uniformity.



(c)	Dielectric constant	D_{it} ($cm^{-2}eV^{-1}$)	Hysteresis (mV)	Leakage currents at -1MV/cm (A/cm^2)
Nanosheet	9.1 (± 1 %)	1.69×10^{11} (± 6 %)	~ 0	7.87×10^{-5} A/cm^2 (± 1 %)
Th-ALD	9.0 (± 1 %)	1.37×10^{12} (± 5 %)	~ 0	2.21×10^{-7} A/cm^2 (± 7 %)

Figure 4. (a) C−V and (b) I−V measurements of the transferred Al_2O_3 nanosheet (30 nm) and Th-ALD Al_2O_3 (30 nm) on the p-type Si substrates (Inset: (a) dielectric constants and interface state densities for 20 devices, (b) leakage currents at −1 MV/cm for 20 devices). (c) Summary of the dielectric properties of 30 nm of Al_2O_3 nanosheet and Th-ALD Al_2O_3.

Top-gated graphene FETs are fabricated with Th-ALD Al_2O_3 directly on graphene for a comparison study of FET using Al_2O_3 NS. Figure 5a shows a schematic of the top-gated graphene FET using Th-ALD Al_2O_3 (left above), the gate electrode/Th-ALD Al_2O_3 /graphene stack (right below) and an SEM image of the Th-ALD Al_2O_3 /graphene (right above). The left below graph of Figure 5a is the Raman spectroscopy of the CVD grown graphene transferred on the SiO_2 substrate, showing typical features of monolayer graphene; ∼0.5 of the G-to-2D intensity ratio, the G band centered at 1593 with a full width at half maximum (FWHM) of 15.1 and the 2D band at 2691 with a FWHM of 33.4.[23,24] The small D peak comes from the transfer process. As shown in the SEM image of Th-ALD 50 nm Al_2O_3/graphene/SiO_2 (Figure 5a, right above), poor coverage of the Al_2O_3 thin films is observed, which is similar to previous reports of poor wetting of Al_2O_3 thin films grown by un-seeded ALD on a monolayer graphene/SiO_2 substrate.[25] The SEM image of Th-ALD Al_2O_3 on the monolayer graphene shows an island-like growth mode resulting in poor wetting of Th-ALD Al_2O_3 on graphene. Figure 5b) shows the drain−source current (I_D) and drain−gate current (I_G) versus gate voltage (V_G) curves of the fabricated device. Large I_G comes from primarily uncovered regions of Th-ALD Al_2O_3 on graphene because of the island-like growth mode (Figure 5a right above) and they make direct connections between the gate electrode and the graphene channel (Figure 5a right below) and produce a large I_G nearly the same as I_D. Nearly all of the I_D flows through the gate electrode (I_G), indicating the Al_2O_3 film by direct Th-ALD on graphene did not work as a gate oxide layer.

Panels a and b in Figure 6 show a schematic representation of the top-gated graphene FET using Al_2O_3 NS and a SEM image of the fabricated top-gated graphene FET, respectively. The electrical transport studies of the top-gated graphene FETs are performed at room temperature. Figure 6c shows the I_D versus drain-source voltage (V_D) output characteristics of the

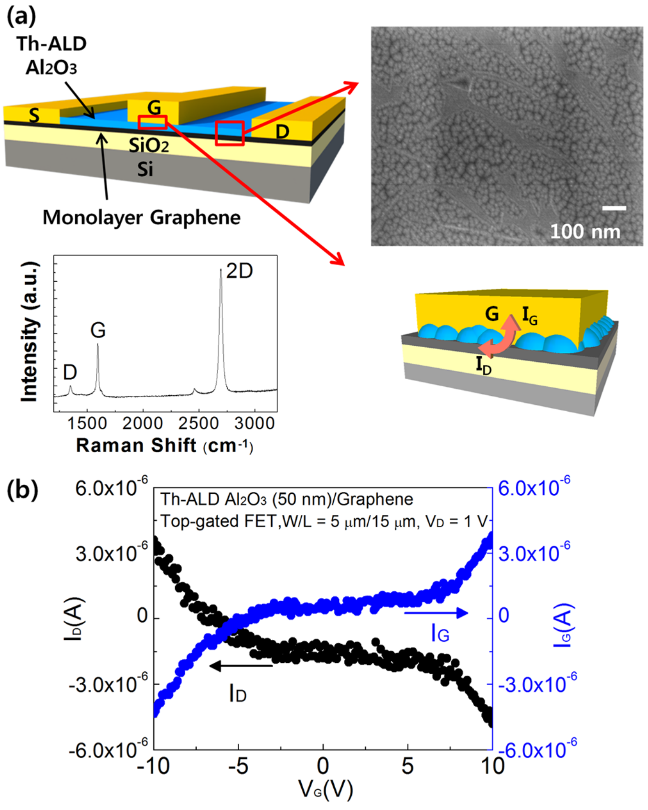


Figure 5. (a) Schematic of the top-gated graphene FET using Th-ALD Al_2O_3 (left), the SEM image of Th-ALD Al_2O_3 on the monolayer graphene (right above) and the schematic of the gate-electrode/Th-ALD Al_2O_3/graphene stack (right below) (Inset: Raman spectrum of monolayer graphene transferred on a 300 nm SiO_2 substrate). (b) Drain−source current (I_D) and drain−gate current (I_G) versus gate voltage (V_G) curves of top-gated graphene FET using Th-ALD Al_2O_3.

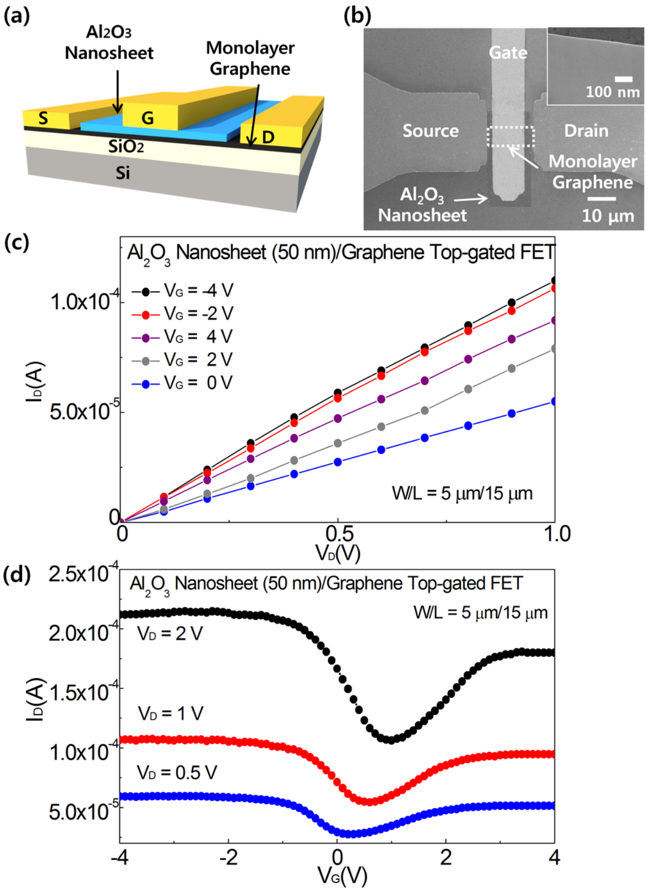


Figure 6. (a) Schematic and (b) SEM image of the top-gated graphene FET using the Al_2O_3 nanosheet (Inset: higher magnification of 50 nm Al_2O_3 nanosheet on graphene). (c) Output curve and (d) transfer curve of fabricated top-gated graphene FET.

FET at various V_G of −4, −2, 0, 2, and 4 V. The device delivers an on-current of 108 μA at V_D = 1 V and V_G = −4 V. The transfer characteristics of the top-gated graphene FET are measured from −4 to +4 V gate bias in Figure 6d. As shown in a family of I_D versus V_G curves with different drain bias V_D values (Figure 6d), the increase in V_D induces the increased overall current and shifts in the curves to the positive voltage direction. This drain-induced Dirac voltage shifting is also observed in previous reports,[26−28] as the drain-induced channel potential weakens the gate control. In ambipolar transistors, the Dirac point, the minimum current point, is reached when the injected electron and hole currents from the source-drain are balanced. Therefore, equal and opposite voltages ($\pm 1/2\ V_D$) to the source and drain are required to hold the Dirac point at a zero gate voltage. Therefore, the gate-source or gate-drain potential difference, which is also the Dirac voltage when either the source or drain is grounded, will shift by $1/2\Delta V_D$ with a change of ΔV_D. In our device, the Dirac voltage shifts approximately 0.7 V when V_D increases from 0.5 to 2 V, close to the theoretical prediction.[26,29,30] The field-effect mobility is extracted based on the slope $(\Delta I_D)/(\Delta V_G)$ fitted to the linear regime of the transfer curves using the equation $\mu = ((\Delta I_D)/(\Delta V_G))(1/(V_D C_{OX})L/W)$ where L and W are the channel length and width, and C_{OX} is the gate oxide capacitance. The extracted field-effect mobilities for the device are ~2200 $cm^2/(V\ s)$ and ~800 $cm^2/(V\ s)$ for the hole and the electron, respectively. The electron-hole asymmetry is originated from the imbalanced carrier injection caused by misalignment between the contact electrode work function and channel neutrality points.[31] Also this asymmetry may come from the residues of PAA on the graphene channel or adsorbent properties of graphene from the open area of channel near the edge of source and drain electrodes where the NS is not attached. These values are larger or similar to other top-gated graphene FETs using plasma-assisted ALD Al_2O_3 directly on graphene (720 $cm^2/(V\ s)$)[10] and transferred gate stacks on graphene (800−2000 $cm^2/(V\ s)$).[17] And the top-gated graphene FET shows good performance with very low leakage currents of ~1.0×10^{-9} A and ~4.1×10^{-10} A at V_G = −5 and 5 V, respectively. Also we did the device stability test and it shows quite stable performance over 1000 times of measurement (see Figure S4 in the Supporting Information).

■ CONCLUSION

A new strategy is demonstrated to integrate graphene with high-quality, physically transferrable Al_2O_3 NS. The Al_2O_3 NS functions as a dielectric layer with a dielectric constant of 9 and zero hysteresis. Additionally, Al_2O_3 NS shows enhanced dielectric properties such as a lower D_{it} value and a smaller flat band voltage shift than Th-ALD Al_2O_3 thin film. Using the Al_2O_3 NS as a gate dielectric, top-gated monolayer graphene FETs are fabricated with excellent performance and high mobilities of 2200 $cm^2/(V\ s)$ and 800 $cm^2/(V\ s)$ for the hole and electron, respectively, which are better than previously reported values. This is a feasible method through which high-performance graphene devices can be fabricated without any chemical or physical treatment on graphene. With further optimization of the NS transfer process and assembly technique, large arrays of top-gated graphene FETs or other physically-assembled electronic devices can be manufactured. Thus, this physically transferrable NS fabrication method can provide a broad, practical approach for high-performance graphene devices and various flexible electronic devices.

■ ASSOCIATED CONTENT

Ⓢ Supporting Information

Further experimental information and stability of devices. This material is available free of charge via the Internet at http://pubs.acs.org/.

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Author Contributions

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Notes

The authors declare no competing financial interest.

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